REMARKS / DISCUSSION OF ISSUES

Claims 1-16 are pending in the application.

The following remarks are being filed in response to the Office Action mailed on November 16, 2006, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

In the Office Action, the Examiner objected to the Abstract for an informality. In response, the prior Abstract has been deleted and substituted with the enclosed New Abstract which corrects the informality noted by the Examiner, and better conforms to U.S. practice. Accordingly, withdrawal of the objection to the Abstract is respectfully requested.

In the Office Action, claims 1 and 2 are rejected under 35 U.S.C. §102(e) as allegedly unpatentable over U.S. Patent Number 6,538,921 (Daughton). Further, claims 3-16 are rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Daughton in view of U.S. Patent Application Publication Number 2006/0216877 (Toyota). It is respectfully submitted that claims 1-16 are patentable over Daughton and Toyota for at least the following reasons.

Daughton is directed to a ferromagnetic thin-film based digital memory circuit. While, the Office Action states on page 5, paragraph 2, and the Applicants agree, that "Daughton fails to teach a specific display application where each pixel of a display is being associated with a respective one of the memory circuits and forms in-pixel memory", it is respectfully submitted that Daughton fails to additionally disclose much of the structural relationships required by the pending claims as discussed in more detail below. Toyota is introduced to allegedly cure the defects of Daughton noted in the Office Action.

The Office Action alleges and the Applicants respectfully refute that Daughton shows elements, such as, "the bit line passes over the first MRAM then turns or meanders back on itself before passing over the second MRAM (Col. 23, Lines 16-51, and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21,62-73)" or " the bit line being arranged to cross over the first MRAM .in a first direction and to cross over the

second MRAM in a second direction, the first direction being substantially opposed to the second direction (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 2 1,62-73)" as alleged on page 4, paragraph continuing onto page 5. In fact, it is respectfully submitted that Col. 23, lines 16-51 describe an interconnection of (emphasis provided) "a flip-flop arrangement ... implementation in CMOS circuitry" (see, Col. 23, lines 18-20) and MOSFET circuitry (see, Col. 23, lines 35-51), not a structural interconnection of an MRAM as required by the claims. Col. 6, lines 31-40 merely describe operation of a MRAM circuit and how either of a one or zero state may be stored in a magnet memory device. While it is not disputed that Daughton shows use of a MRAM, it is respectfully submitted that the currently pending claims may not be read so broadly since particular structural relationships are recited in the claims that are not disclosed in the cited prior art.

Toyota is directed to a dynamic random access memory (DRAM) based image display having gate-lines and signal-lines supporting a pixel as shown in the circuit diagram FIG. 28. As shown in FIG. 28, the pixel in the upper right corner consists of a data input switch 221, a pixel electrode 224, and a storage capacitor 222 which is connected to common electrode driver circuit 237 (see FIG. 28).

While the Office Action cites sections of Toyota for showing MRAM (e.g., see Office Action, page 5, lines 10-12), it is respectfully submitted that no such MRAM is disclosed within these sections. Even presuming arguendo that MRAM may be substituted in Toyota, this still is not sufficient to render obvious the specific structural relationships recited in each of the currently pending claims. While sections of Toyota are recited for showing these limitations, it is respectfully submitted that the recited sections are not relevant to the claim limitations.

For example, while FIG. 28 is recited for showing "a bit line, the bit line running from the switching device to the pixel electrode (pages 7 and 8, paragraph 92, see figure 28, items 221,22 and 230, page 9, paragraph 110); the bit line connects with a respective one end of each of the first and second MRAMs; and further comprising: a word line, running under the other ends of each of the first and

second MRAMs, for addressing the MRAMs; and a gate line, for driving the switching device, coupled to the switching device; the word line being arranged between the pixel electrode and the gate line such that the bit line passes over the word line but does not pass over the gate line (pages 7 and 8, paragraph 92., figure 28, items 221,22 and 230, page 9, paragraph 110 and page 8, paragraphs 93,94, page 7, paragraphs 85-91)". It is respectfully submitted that none of these recited sections, with the exception of paragraphs 93-94, actually shows structural portions of the elements. In fact, FIG. 28 for example merely shows an interconnection of the elements in a circuit diagram. While paragraphs 93-94 and FIG. 30 does show a structure of a DRAM, it is not the structure required by the claims.

Therefore, it is respectfully is respectfully submitted that Daughton and Toyota, alone or in combination, do not disclose or suggest the present invention as recited in independent claim 7, and similarly recited in independent claims 1 and 4 which, amongst other patentable elements, requires (illustrative emphasis provided): "the bit line being arranged to cross over the first MRAM in a first direction and to cross over the second MRAM in a second direction, the first direction being substantially opposed to the second direction."

Further, Toyota does not disclose nor suggest how to distinguish, presuming their existence in Toyota, between a bit line, a word line and a gate line, let alone the physical interrelationship amongst them, as required by claim 10 of the present application. None of these terms are specifically recited in Toyota or identified by the Office Action.

Therefore, it is further respectfully submitted that Daughton and Toyota, alone or in combination, do not disclose or suggest (illustrative emphasis provided): "a bit line running from the switching device to the pixel electrode via one end of each of the one or more MRAMs; a word line, running under the other ends of each of the one or more MRAMs, for addressing the MRAMs; and a gate line, for driving the switching device, coupled to the switching device; the word line being arranged between the pixel electrode and the gate line such that the bit line passes over the word line but does not pass over the gate line" as required by claim 10.

Further, there is no disclosure or suggestion in Toyota of a method of forming an in-pixel memory display device wherein the word line and the gate line are formed during a same masking stage as required by claim 13, nor wherein the bit line and the column line are formed during a same masking stage as required by claim 14.

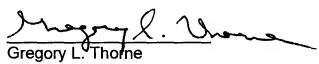
This is simply not shown in Daulton, Toyota, or combination thereof. For example, while FIG. 9 of Toyota shows a gate electrode 7/gate line and a storage electrode 8 (see, paragraph [0051]), the structure required by claims 13 and 14 is simply not shown.

Accordingly, it is respectfully submitted that independent claims 1, 4, 7, 10, 13, and 14 should be allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 2-3, 5-6, 8-9, 11-12 and 15-16 should also be allowed at least based on their dependence from independent claims 1, 4, 7, 10, 13 and 14, as well as for the separately patentable elements contained in each of the dependent claims. Accordingly, separate consideration and allowance of each of the dependent claims is respectfully requested.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the foregoing, Applicants respectfully request that the Examiner withdraw the rejections of record, allow all the pending claims, and find the application in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,



Gregory L. Thorne
Reg. 39,398
Attorney for Applicant(s)
February 16, 2007

THORNE & HALAJIAN, LLP
Applied Technology Center
111 West Main Street
Phone: (631) 665-5139
Fax: (631) 665-5101